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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,371	12/07/2001	Leith Johnson	10016615-1	8105

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EXAMINER

TSAI, SHENG JEN

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/017,371

Applicant(s)

JOHNSON, LEITH

Examiner

Sheng-Jen Tsai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 8-11, 14-21, 23, 25 and 27-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8-11, 14-21, 23, 25 and 27-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Appeal Brief filed on October 4, 2006 regarding application 10/017,371 filed on December 7, 2001.
2. Claims 1-5, 8-11, 14-21, 23, 25 and 27-31 are pending for consideration.
3. **Reopening of Prosecution After Appeal Brief**

In view of the Appeal Brief filed on October 4, 2006, PROSECUTION IS HEREBY REOPENED as set forth below.

A new ground of claim analysis based on a previously identified reference (Vishin et al., US-5,860,146) has been embarked. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 8-11, 14-21, 23, 25 and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Vishin et al. (US 5,860,146).

As to claim 1, Vishin et al. disclose **in a partitionable computer system** [figure 1 shows a partitionable computer system: the computer system is partitioned into a plurality of clusters (102), and each cluster is further partitioned into a plurality of processing unit (104)] **including a plurality of machine resources having a plurality of machine resource identifiers** [figure 1 shows a partitionable computer system: the

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computer system is partitioned into a plurality of clusters (102), and each cluster is further partitioned into a plurality of processing unit (104); each of the plurality of clusters represent a plurality of machine resources (i.e., nodes) with machine resource identifier (the Node-ID, figure 7, 170)], **a method for creating a physical resource identifier space in a partition of the partitionable computer system** [the corresponding physical resource identifier space is the Remote Translation Lookaside Table (RTLb, figure 8, 160) which is used to derive the Remote Page Physical Address (figure 6, 168; figure 7) that is then used to access Remote Physical Address (figure 5) associated with the plurality of clusters (figure 1, 102); abstract], **the method comprising steps of:**

(A) **establishing a mapping** [figures 2-8 show the mapping; abstract] **between a plurality of physical resource identifiers** [the RTLb, figure 8, 160] **and at least some of the plurality of machine resource identifiers** [Node-ID (figure 7, 170) and the associated Remote Physical Address (figure 7, 172)], **wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero** [figure 8, 160 shows that the RTLb includes a plurality of RPTE entries that are numbered sequentially beginning with 0]; **and wherein the mapping defines a non-monotonic function** [figure 8 shows that the mapping from the RPTE to the Remote Physical Address is non-monotonic, because the RPTE of entry #1 is mapped into the slashed area (the file and DB segment locked by local processor) located in the middle of the Remote Physical Address Space while the RPTE of entry #8 is mapped into

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areas of the Remote Physical Address Space both “above” and “below” that of the RPTE of entry #1. Thus this mapping is clearly non-monotonic]; and

(B) **providing, to an operating system executing in the partition** [In response to the page fault the operating system of the cluster 102 will request the memory controller 112 to retrieve the specified page from secondary memory 110 and store it in a free page in primary memory 108 (column 2, lines 36-40)], **an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource identifiers as indices into the content address memory** [The 32 entries in the RTLb are organized into four groups of eight entries (entries 0:7, 8:15, 16:23 and 24:31). While the physical address ranges of the RPTEs in any one group may overlap, it is the responsibility of the operating system 180 (see FIG. 9) to make sure that the RPTEs in different groups do not have overlapping address ranges (column 5, lines 33-59)].

As to claim 2, Vishin et al. disclose that **the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses], and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses** [figure 7 shows Node-ID (figure 7, 170) and the associated Remote Physical Address (figure 7, 172); figures 1-8 illustrate the mapping into the physical address associated with the plurality of machine resources (the clusters, figure 1, 102)].

As to claim 3, Vishin et al. disclose that **the method of claim 1 further comprising a step of performing the steps (A) and (B) for each of a plurality of partitions of the partitionable computer** [figure 7 shows Node-ID (figure 7, 170) and the associated Remote Physical Address (figure 7, 172); figures 1-8 illustrate the mapping into the physical address associated with the plurality of machine resources (the clusters, figure 1, 102)].

As to claim 4, Vishin et al. disclose that **the step (A) comprises a step of creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers** [the Remote Translation Lookaside Table (RTL, figure 8, 160) which is used to derive the Remote Page Physical Address (figure 6, 168; figure 7) that is then used to access Remote Physical Address (figure 5) associated with the plurality of clusters (figure 1, 102); abstract].

As to claim 5, Vishin et al. disclose that **the interface comprises means for translating a physical resource identifier selected from among the plurality of physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping** [the Remote Translation Lookaside Table (RTL, figure 8, 160) which is used to derive the Remote Page Physical Address (figure 6, 168; figure 7) that is then used to access Remote Physical Address (figure 5) associated with the plurality of clusters (figure 1, 102); abstract].

As to claim 8, refer to "As to claim 1."

As to claim 9, refer to "As to claim 2."

As to claim 10, refer to "As to claim 4."

As to claim 11, refer to "As to claim 5."

As to claim 14, refer to "As to claim 1" through "As to claim 5." Further, Vishin et al. disclose that [Each remote page table entry represents a mapping between a range of physical addresses and a corresponding range of remote physical addresses. The primary translation lookaside buffer translates a virtual address asserted by the data processor into a physical address. When the physical address does not correspond to a location in the local memory, the RTLB determines whether the physical address matches at least one of the remote page table entries stored in the RTLB, and selects one of those remote page table entries when at least one match is found. The RTLB's selection circuitry selects a single remote page table entry in accordance with predefined RPTE selection criteria when two or more of the remote page table entries match the physical address. Then, a remote physical address is generated by combining a portion of the selected remote page table entry with a portion of the physical address (abstract); The present invention relates generally to multiprocessor computer systems having virtual memory management subsystems, and particularly to a memory controller that manages access to remote physical addresses through the use of an auxiliary translation lookaside buffer (column 1, lines 5-10)].

As to claim 15, refer to "As to claim 2."

As to claims 16-17, Vishin et al. disclose that [For instance, the control flags 176 may be used to indicate "read only" access or "read/write" access to the specified remote memory block (column 7, lines 48-53)].

As to claim 18, refer to "As to claim 14."

As to claim 19, refer to "As to claim 2."

As to claims 20-21, refer to "As to claims 16-17."

As to claim 23, refer to "As to claim 1" through "As to claim 5." Further, Vishin et al. disclose

(A) selecting a first subset of the plurality of physical memory locations, the first subset of the plurality of memory locations being mapped to a first subset of the plurality of machine memory addresses [When the physical address does not correspond to a location in the local memory, the RTLB determines whether the physical address matches at least one of the remote page table entries stored in the RTLB, and selects one of those remote page table entries when at least one match is found. The RTLB's selection circuitry selects a single remote page table entry in accordance with predefined RPTE selection criteria when two or more of the remote page table entries match the physical address. Then, a remote physical address is generated by combining a portion of the selected remote page table entry with a portion of the physical address (abstract)]; **and**

(B) copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses [If the cluster's memory 108 does not store the page of the remote page table containing the required RPTE, that page of the remote page table 150 will first need to be downloaded from an appropriate remotely located processor or cluster in the distributed system 100. Once the required RPTE 152 is found and the address

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translation into a remote physical address (RPA) is performed, then a request is transmitted via the network 114 to load a copy of the page being addressed into the requesting cluster's local memory 108 (column 3, lines 22-30)].

As to claim 25, refer to "As to claim 23."

As to claim 27, Vishin et al. teach that **the interface comprises a Content Addressable Memory that establishes the mapping** [figure 6, 162 shows that a CAM is used to implement a remote translation lookaside buffer (RTLB); column 4, lines 63-67; column 5, lines 1-20, and the association of the physical resource identifiers and the indices of the CAM (figure 6; column 5, lines 60-67; column 4, lines 5-10; column 5, lines 32-59; column 6, lines 1-35)].

As to claim 28, refer to "As to claim 27."

As to claim 29, refer to "As to claim 27."

As to claim 30, Vishin et al. teach **copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses** [If the cluster's memory 108 does not store the page of the remote page table containing the required RPTE, that page of the remote page table 150 will first need to be downloaded from an appropriate remotely located processor or cluster in the distributed system 100. Once the required RPTE 152 is found and the address translation into a remote physical address (RPA) is performed, then a request is transmitted via the network 114 to load a copy of the page being addressed into the requesting cluster's local memory 108 (column 3, lines 22-30)].

As to claim 31, refer to "As to claim 30."

6. *Related Prior Art*

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Gulick et al., (US 6,314,501), "Computer System and Method for Operating Multiple Operating Systems in Different Partitions of the Computer System and for Allowing the Different Partitions to Communicate with One Another through Shared Memory."
- Kirk, (US 5,875,464), "Computer System with Private and Shared partition in Cache."
- Van Doren, (US Patent Application Publication 2001/0037435), "Distributed Address Mapping and Routing Table Mechanism That Supports Flexible Configuration and Partitioning in a Modular Switch-Based Shared-memory Multiprocessor Computer System."
- Chi et al., (US 5,940,870), "Address Translation for Shared-memory Multiprocessor Clustering."
- Greenstein et al., (US 5,784,702), "System and method for Dynamically Performing Resource Reconfiguration in a Logically Partitioned Data Processing System."
- White et al., (US 5,721,858), "Virtual Memory Mapping Method and System for memory Management of pools of Logical Partitions for BAT and TLB Entries in a Data Processing System."

- Huber et al., (US 5,455,775), "Computer Design System for Mapping a Logical Hierarchy into a Physical Hierarchy."
- Parrish et al., (US 5,117,350), "Memory Address Mechanism in a Distributed memory Architecture."
- George et al., (US 4,51,964), "Dynamic Physical Memory Mapping and Management of Independent Programming Environments."
- Alvarez et al., (US 3,723,976), "Memory system with Logical and Real Addressing."

Conclusion


7. Claims 1-5, 8-11, 14-21, 23, 25 and 27-31 are rejected as explained above.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

November 6, 2006


PIERRE BATAILLE
PRIMARY EXAMINER
11/03/06